other elements of the semiconductor device illustrated in FIGS. **2**A, **14**, **15**A, and **15**B will be omitted.

[0110] The MOSFET region MR may include a PMOSFET region PR and an NMOSFET region NR. The PMOSFET region PR and the NMOSFET region NR may be spaced apart from each other in the second direction D**2**. The PMOSFET region PR may be the substantially same as the MOSFET region MR of FIGS. **1** and **2**A to **2**C which is the PMOSFET region, and the NMOSFET region NR may be the substantially same as the MOSFET region MR of FIGS. **1** and **2**A to **2**C which is the NMOSFET region.

[0111] The gate separation pattern GS may include first, second, and third gate separation patterns GS**1**, GS**2**, and GS**3** spaced apart from each other. Each of the first, second, and third gate separation patterns GS**1**, GS**2**, and GS**3** may be the substantially same as the gate separation pattern GS described with reference to FIGS. **1** and **2**A to **2**C.

[0112] The first gate separation pattern GS**1** and the second gate separation pattern GS**2** may be spaced apart from each other with the MOSFET region MR interposed therebetween when viewed from a plan view. The first gate separation pattern GS**1** may be adjacent to the PMOSFET region PR, and the second gate separation pattern GS**2** may be adjacent to the NMOSFET region NR. The first gate separation pattern GS**1** may have a tensile strain, and the second gate separation pattern GS**2** may have a compressive strain. Thus, the first gate separation pattern GS**1** may apply a compressive strain to the active patterns AP of the PMOSFET region PR, and the second gate separation pattern GS**2** may apply a tensile strain to the active patterns AP of the NMOSFET region NR. As described above, the influence (e.g., the strain) of the gate separation pattern GS on other elements adjacent thereto may decrease as a distance from the gate separation pattern GS increases. Thus, the compressive strain applied to the active patterns AP of the NMOSFET region NR by the first gate separation pattern GS**1** may be relatively small, and the tensile strain applied to the active patterns AP of the PMOSFET region PR by the second gate separation pattern GS**2** may also be relatively small. As a result, improving characteristics of transistors formed on the PMOSFET region PR and characteristics of transistors formed on the NMOSFET region NR may be possible.

[0113] The third gate separation pattern GS**3** may be provided between the PMOSFET region PR and the NMOSFET region NR when viewed from a plan view. The third gate separation pattern GS**3** may have a tensile strain or a compressive strain.

[0114] According to some example embodiments, a distance between the third gate separation pattern GS**3** and the PMOSFET region PR may be less than a distance between the third gate separation pattern GS**3** and the NMOSFET region NR when viewed from a plan view. In this case, the third gate separation pattern GS**3** may have the tensile strain. As described above, the influence (e.g., the strain) of the gate separation pattern GS on other elements adjacent thereto may decrease as a distance from the gate separation pattern GS increases. Thus, a magnitude of a compressive strain applied to the NMOSFET region NR by the third gate separation pattern GS**3** may be less than that of a compressive strain applied to the PMOSFET region PR by the third gate separation pattern GS**3**.

[0115] According to some example embodiments, the distance between the third gate separation pattern GS**3** and the NMOSFET region NR may be less than the distance between the third gate separation pattern GS**3** and the PMOSFET region PR when viewed from a plan view. In this case, the third gate separation pattern GS**3** may have the compressive strain.

[0116] Thus, a magnitude of a tensile strain applied to the PMOSFET region PR by the third gate separation pattern GS**3** may be less than that of a tensile strain applied to the NMOSFET region NR by the third gate separation pattern GS**3**.

[0117] As a result, further improvement to the characteristics of the transistors formed on the PMOSFET region PR or the characteristics of the transistors formed on the NMOSFET region NR may be possible.

[0118] According to some example embodiments of the inventive concepts, the strain applied to the active pattern adjacent to the gate separation pattern may be adjusted by the gate separation pattern, and thus, improving the characteristics of the transistor adjacent to the gate separation pattern may be possible.

[0119] According to some example embodiments of the inventive concepts, the strain applied to the gate electrode adjacent to the gate separation pattern may be adjusted by the gate separation pattern, and thus, it is possible to adjust the concentration of the impurities (e.g., oxygen or fluorine) contained in the gate electrode. As a result, the work function of the gate electrode may be adjusted.

[0120] While the inventive concepts have been described with reference to example embodiments, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the spirits and scopes of the inventive concepts. Therefore, it should be understood that the above embodiments are not limiting, but illustrative. Thus, the scopes of the inventive concepts are to be determined by the broadest permissible interpretation of the following claims and their equivalents, and shall not be restricted or limited by the foregoing description.

What is claimed is:

1. A semiconductor device comprising:

a substrate including at least one metal-oxide-semiconductor field-effect transistor (MOSFET) region defined by a device isolation layer, the substrate having an active pattern extending in a first direction on the MOSFET region;

a gate electrode intersecting the active pattern on the substrate, the gate electrode extending in a second direction intersecting the first direction; and

a first gate separation pattern adjacent to the MOSFET region when viewed from a plan view, the first gate separation pattern dividing the gate electrode into segments spaced apart from each other in the second direction, the first gate separation pattern having one of a tensile strain and a compressive strain when the MOSFET region is one of a P-channel MOSFET (PMOSFET) and a N-channel MOSFET (NMOSFET), respectively.

2. The semiconductor device of claim **1**, wherein

the MOSFET region is the PMOSFET region; and

the active pattern has a compressive strain.

3. The semiconductor device of claim **1**, wherein

the MOSFET region is the NMOSFET region; and

the active pattern has a tensile strain.

4. The semiconductor device of claim **1**, wherein a bottom surface of the first gate separation pattern is at a lower level than a bottom surface of the gate electrode.